

# LM5010

## High Voltage 1A Step Down Switching Regulator

### General Description

The LM5010 Step Down Switching Regulator features all the functions needed to implement a low cost, efficient, buck bias regulator capable of supplying in excess of 1A load current. This high voltage regulator contains an N-Channel Buck Switch, and is available in thermally enhanced LLP-10 and TSSOP-14EP packages. The hysteretic regulation scheme requires no loop compensation, results in fast load transient response, and simplifies circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection is set at 1.25A. Additional features include:  $V_{CC}$  under-voltage lockout, thermal shutdown, gate drive under-voltage lockout, and maximum duty cycle limiter.

### Features

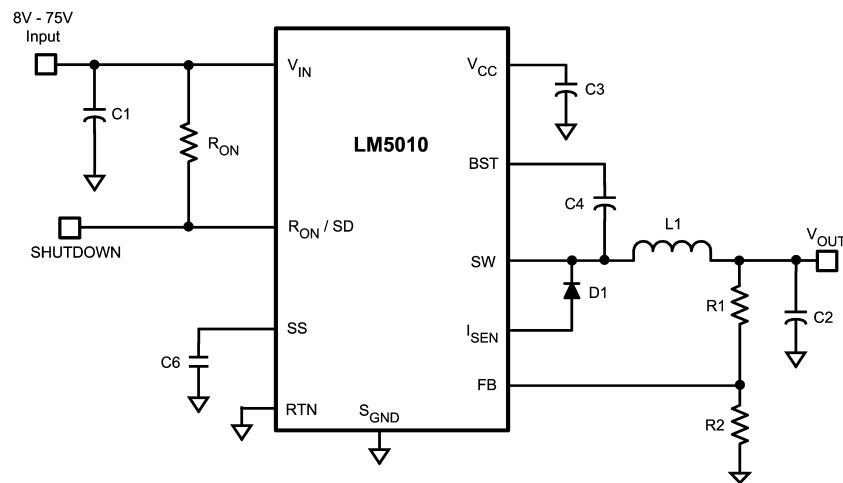
- Input Voltage Range: 8V to 75V
- Valley Current Limit At 1.25A
- Switching Frequency Can Exceed 1 MHz
- Integrated N-Channel Buck Switch
- Integrated Startup Regulator
- No Loop Compensation Required
- Ultra-Fast Transient Response
- Operating Frequency Remains Constant With Load and Line Variations
- Maximum Duty Cycle Limited During Startup
- Adjustable Output Voltage
- Precision 2.5V Feedback Reference
- Thermal shutdown

### Typical Applications

- High Efficiency Point-Of-Load (POL) Regulator
- Non-Isolated Telecommunications Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems

### Package

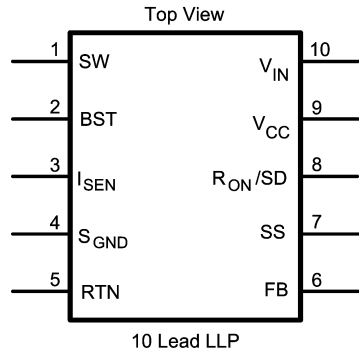
- LLP-10 (4 mm x 4 mm)
- TSSOP-14EP
- Both Packages Have Exposed Thermal Pad For Improved Heat Dissipation



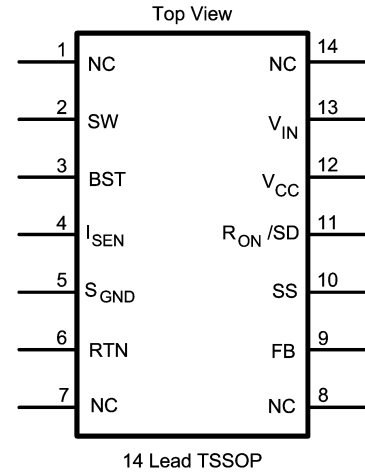
Basic Stepdown Regulator

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## Connection Diagrams



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## Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5010SD	LLP-10 (4x4)	SDC10A	1000 Units on Tape and Reel
LM5010SDX	LLP-10 (4x4)	SDC10A	4500 Units on Tape and Reel
LM5010MH	TSSOP-14EP	MXA14A	94 Units in Rail
LM5010MHX	TSSOP-14EP	MXA14A	2500 Units on Tape and Reel

## Pin Description

PIN NUMBER		NAME	DESCRIPTION	APPLICATION INFORMATION
LLP-10	TSSOP-14			
1	2	SW	Switching Node	Internally connected to the buck switch source. Connect to the inductor, free-wheeling diode, and bootstrap capacitor.
2	3	BST	Boost pin for bootstrap capacitor	Connect a 0.022 $\mu$ F capacitor from SW to this pin. The capacitor is charged from $V_{CC}$ via an internal diode during each off-time.
3	4	$I_{SEN}$	Current sense	The re-circulating current flows through the internal sense resistor, and out of this pin to the free-wheeling diode. Current limit is nominally set at 1.25A.
4	5	$S_{GND}$	Sense Ground	Re-circulating current flows into this pin to the current sense resistor.
5	6	RTN	Circuit Ground	Ground for all internal circuitry other than the current limit detection.
6	9	FB	Feedback input from the regulated output	Internally connected to the regulation and over-voltage comparators. The regulation level is 2.5V.
7	10	SS	Softstart	An internal 11.5 $\mu$ A current source charges an external capacitor to 2.5V, providing the softstart function.
8	11	$R_{ON}/SD$	On-time control and shutdown	An external resistor from $V_{IN}$ to this pin sets the buck switch on-time. Grounding this pin shuts down the regulator.
9	12	$V_{CC}$	Output from the startup regulator	Nominally regulates at 7.0V. An external voltage (7.5V-14V) can be applied to this pin to reduce internal dissipation. An internal diode connects $V_{CC}$ to $V_{IN}$ .
10	13	$V_{IN}$	Input supply voltage	Nominal input range is 8.0V to 75V.
	1,7,8,14	NC	No connection.	No internal connection.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_{IN}$ to GND	76V
BST to GND	90V
SW to GND (Steady State)	-1.5V
BST to $V_{CC}$	76V
BST to SW	14V
$V_{CC}$ to GND	14V
$S_{GND}$ to RTN	-0.3V to +0.3V
SS to RTN	-0.3V to 4V

$V_{IN}$ to SW	76V
Current Out of $I_{SEN}$	See Text
All Other Inputs to GND	-0.3 to 7V
ESD Rating (Note 2)	
Human Body Model	2kV
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering 4 sec) (Note 4)	260°C

**Operating Ratings** (Note 1)

$V_{IN}$	8V to 75V
Operating Junction Temperature	-40°C to + 125°C

**Electrical Characteristics**

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and those with **boldface** type apply over full **Operating Junction Temperature range**.  $V_{IN} = 48\text{V}$ ,  $R_{ON} = 200\text{k}\Omega$ , unless otherwise stated (Note 5) and (Note 6).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b><math>V_{CC}</math> Regulator</b>						
$V_{CCReg}$	$V_{CC}$ regulated output		<b>6.6</b>	7	<b>7.4</b>	Volts
	$V_{IN} - V_{CC}$	$I_{CC} = 0\text{ mA}$ , $F_S < 200\text{ kHz}$ $7.5\text{V} \leq V_{IN} \leq 8.0\text{V}$		1.3		V
	$V_{CC}$ output impedance ( $0\text{ mA} \leq I_{CC} \leq 5\text{ mA}$ )	$V_{IN} = 8.0\text{V}$ $V_{IN} = 48\text{V}$		140 2.5		$\Omega$
	$V_{CC}$ current limit (Note 3)	$V_{CC} = 0\text{V}$		10		mA
$UVLO_{VCC}$	$V_{CC}$ under-voltage lockout threshold	$V_{CC}$ increasing		5.8		V
	$UVLO_{VCC}$ hysteresis	$V_{CC}$ decreasing		145		mV
	$UVLO_{VCC}$ filter delay	100 mV overdrive		3		$\mu\text{s}$
	$I_{IN}$ operating current	Non-switching, $FB = 3\text{V}$		650	<b>850</b>	$\mu\text{A}$
	$I_{IN}$ shutdown current	$R_{ON}/SD = 0\text{V}$		95	<b>200</b>	$\mu\text{A}$
<b>Switch Characteristics</b>						
$R_{ds(on)}$	Buck Switch $R_{ds(on)}$	$I_{TEST} = 200\text{ mA}$		0.35	<b>0.80</b>	$\Omega$
$UVLO_{GD}$	Gate Drive UVLO	$V_{BST} - V_{SW}$ Increasing	<b>3.0</b>	4.3	<b>5.0</b>	V
	$UVLO_{GD}$ hysteresis			440		mV
<b>Softstart Pin</b>						
	Pull-up voltage			2.5		V
	Internal current source			11.5		$\mu\text{A}$
<b>Current Limit</b>						
$I_{LIM}$	Threshold	Current out of $I_{SEN}$	<b>1</b>	1.25	<b>1.5</b>	A
	Resistance from $I_{SEN}$ to $S_{GND}$			130		$\text{m}\Omega$
	Response time			150		ns
<b>On Timer, <math>R_{ON}/SD</math> Pin</b>						
$t_{ON-1}$	On-time	$V_{IN} = 10\text{V}$ , $R_{ON} = 200\text{ k}\Omega$	<b>2.1</b>	2.75	<b>3.4</b>	$\mu\text{s}$
$t_{ON-2}$	On-time	$V_{IN} = 75\text{V}$ , $R_{ON} = 200\text{ k}\Omega$	<b>290</b>	390	<b>490</b>	ns
	Shutdown threshold	Voltage at $R_{ON}/SD$ rising	<b>0.35</b>	0.65	<b>1.1</b>	V
	Threshold hysteresis	Voltage at $R_{ON}/SD$ falling		40		mV
<b>Off Timer</b>						
$t_{OFF}$	Off-time			265		ns

## Electrical Characteristics (Continued)

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and those with **boldface** type apply over full **Operating Junction Temperature range**.  $V_{IN} = 48\text{V}$ ,  $R_{ON} = 200\text{k}\Omega$ , unless otherwise stated (Note 5) and (Note 6).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Regulation and Over-Voltage Comparators (FB Pin)</b>						
$V_{REF}$	FB regulation threshold	SS pin = steady state	<b>2.445</b>	2.5	<b>2.550</b>	V
	FB over-voltage threshold			2.9		V
	FB bias current			1		nA
<b>Thermal Shutdown</b>						
$T_{SD}$	Thermal shutdown temperature			175		$^\circ\text{C}$
	Thermal shutdown hysteresis			20		$^\circ\text{C}$
<b>Thermal Resistance</b>						
$\theta_{JA}$	Junction to Ambient	SDC Package MXA Package		40 40		$^\circ\text{C/W}$

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

**Note 2:** The human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin.

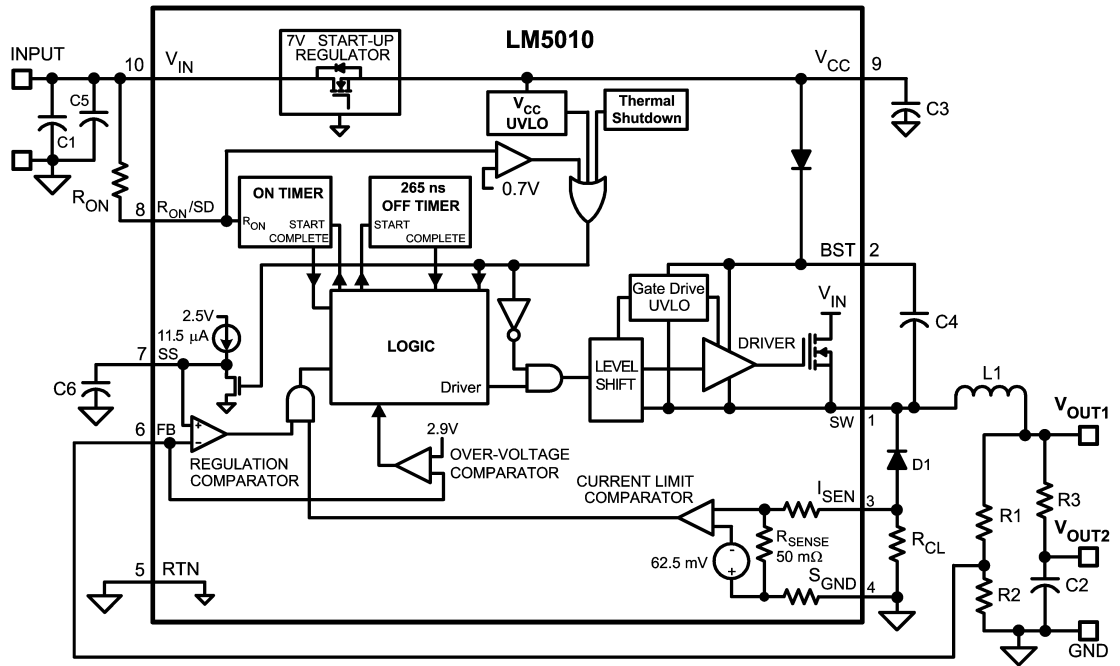
**Note 3:**  $V_{CC}$  provides bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

**Note 4:** For detailed information on soldering plastic TSSOP and LLP packages refer to the Packaging Data Book available from National Semiconductor Corporation.

**Note 5:** Typical specifications represent the most likely parametric norm at 25 $^\circ\text{C}$  operation.

**Note 6:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with  $T_A = 25^\circ\text{C}$ . All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

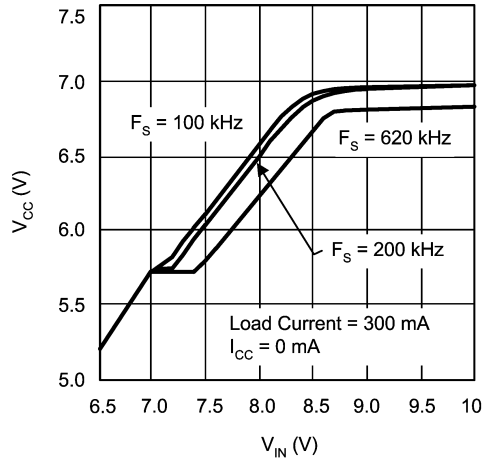
Typical Application Circuit and Block Diagram  
(pin numbers are for the LLP-10 package)



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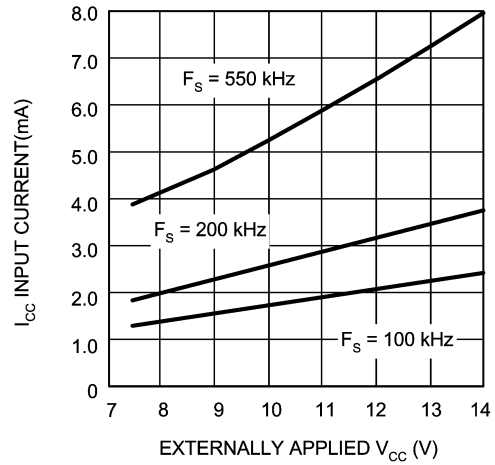
FIGURE 1.

# Typical Performance Characteristics



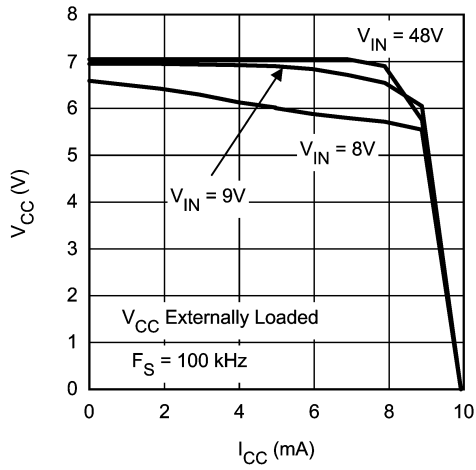
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FIGURE 2.  $V_{CC}$  vs  $V_{IN}$



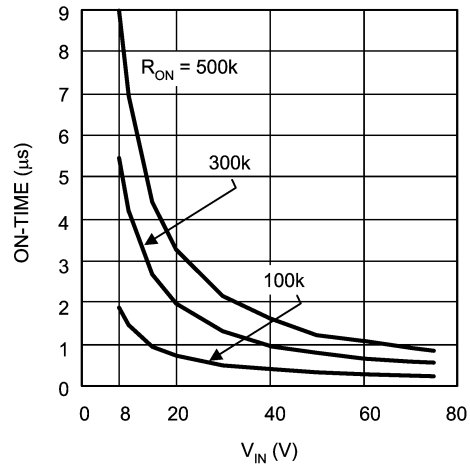
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FIGURE 4.  $I_{CC}$  vs Externally Applied  $V_{CC}$



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FIGURE 3.  $V_{CC}$  vs  $I_{CC}$



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FIGURE 5. On-Time vs  $V_{IN}$  and  $R_{ON}$

**Typical Performance Characteristics** (Continued)

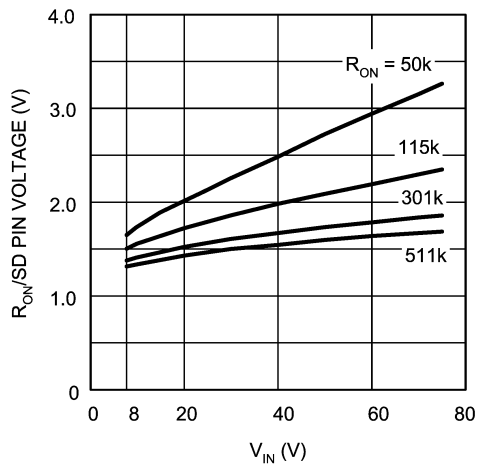


FIGURE 6. Voltage at R<sub>ON</sub>/SD Pin

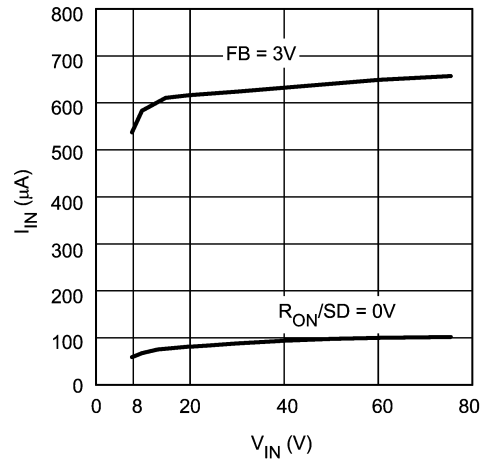
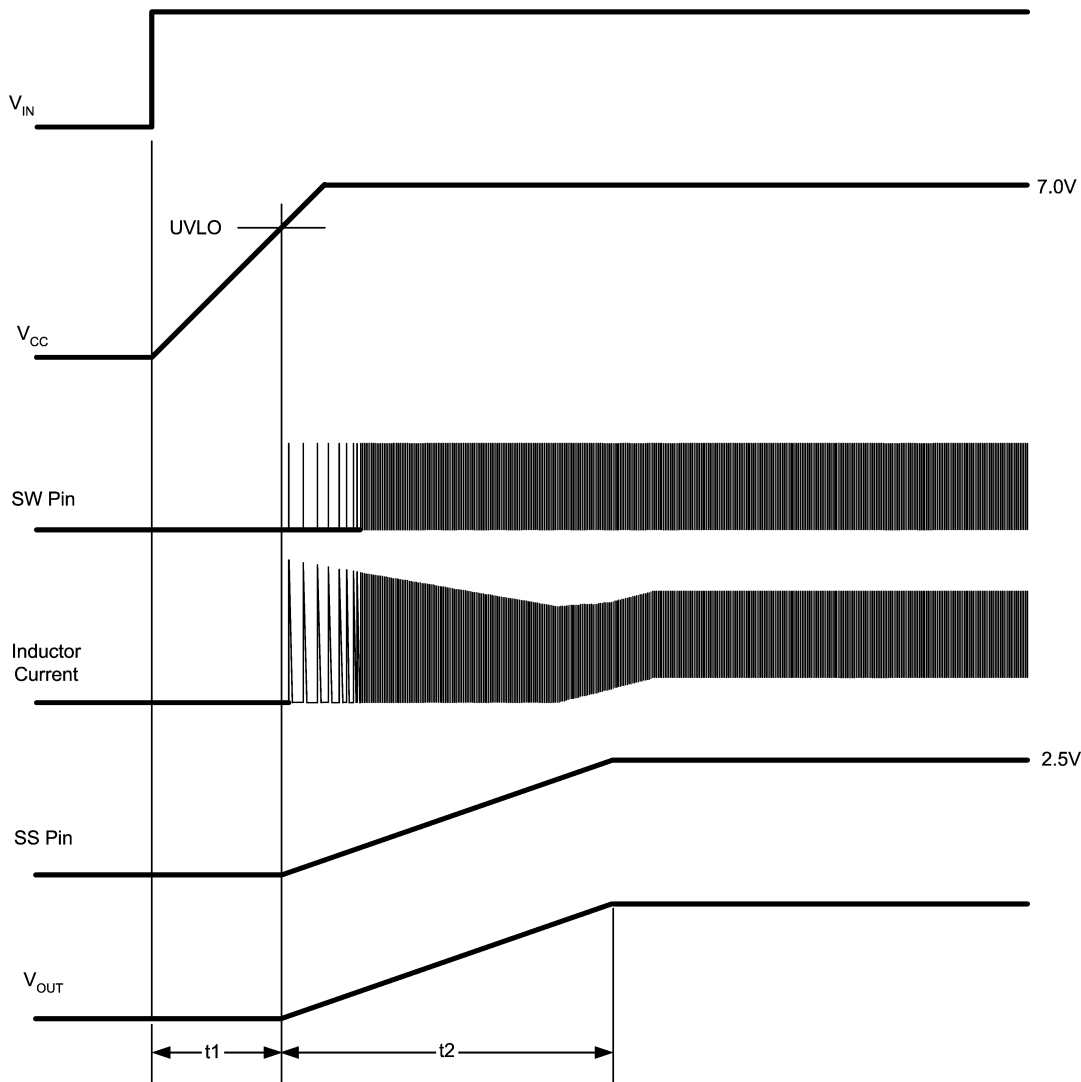


FIGURE 7. I<sub>IN</sub> vs V<sub>IN</sub>



## Typical Performance Characteristics (Continued)



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FIGURE 8. Startup Sequence

### Functional Description

The LM5010 Step Down Switching Regulator features all the functions needed to implement a low cost, efficient buck bias power converter capable of supplying in excess of 1A to the load. This high voltage regulator contains an N-Channel buck switch, is easy to implement, and is available in the thermally enhanced LLP-10 and TSSOP-14EP packages. The regulator's operation is based on a hysteretic control scheme, and uses an on-time which varies inversely with  $V_{IN}$ . This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The switching frequency can range from 100 kHz to > 1.0 MHz. The hysteretic control requires no loop compensation resulting in very fast load transient response. The valley current limit detection circuit, internally set at 1.25A, holds the buck switch off until the high current level subsides. *Figure 1* shows the functional block diagram. The LM5010 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for

48V telecom applications, as well as the new 42V automotive power bus. Implemented as a Point-of-Load regulator following a highly efficient intermediate bus converter can result in high overall system efficiency. Features include: Thermal shutdown,  $V_{CC}$  under-voltage lockout, gate drive under-voltage lockout, and maximum duty cycle limit.

### Hysteretic Control Circuit Overview

The LM5010 buck DC-DC regulator employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.5V). If the FB voltage is below the reference the buck switch is turned on for a time period determined by the input voltage and a programming resistor ( $R_{ON}$ ). Following the on-time the switch remains off for 265 ns, or until the FB voltage falls below the reference, whichever is longer. The buck switch then turns on for another on-time period.

## Hysteretic Control Circuit Overview

(Continued)

Typically when the load current increases suddenly, the off-times are temporarily at the minimum of 265 ns. Once regulation is established, the off-time resumes its normal value. The output voltage is set by two external resistors (R1, R2). The regulated output voltage is calculated as follows:

$$V_{OUT} = 2.5V \times (R1 + R2) / R2 \quad (1)$$

Output voltage regulation is based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. The LM5010 requires a minimum of 25 mV of ripple voltage at the FB pin. In cases where the capacitor's ESR is insufficient additional series resistance may be required (R3 in *Figure 1*).

When in regulation, the LM5010 operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode current always flows through the inductor, never reaching zero during the off-time. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The approximate operating frequency is calculated as follows:

$$F_s = \frac{V_{OUT}}{1.18 \times 10^{-10} \times R_{ON}} \quad (2)$$

The buck switch duty cycle is approximately equal to:

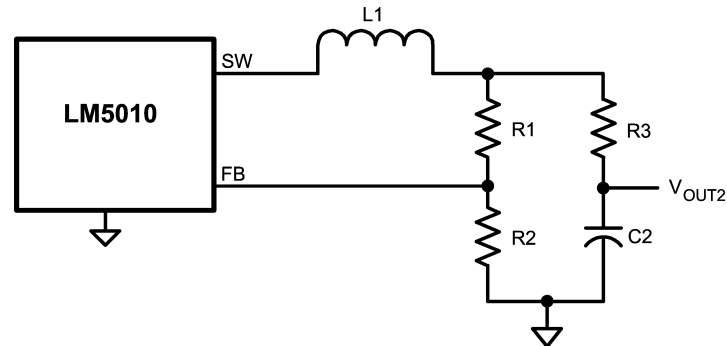
$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

At low load current, the circuit operates in discontinuous conduction mode, during which the inductor current ramps up from zero to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the reference - until then the inductor current remains zero, and the load current is supplied by the output capacitor (C2). In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained at light loads since the switching losses reduce with the reduction in load and frequency. The approximate discontinuous operating frequency can be calculated as follows:

$$F_s = \frac{V_{OUT}^2 \times L1 \times 1.4 \times 10^{20}}{R_L \times (R_{ON})^2} \quad (4)$$

where  $R_L$  = the load resistance.

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor as shown in *Figure 9*. However, R3 slightly degrades the load regulation.



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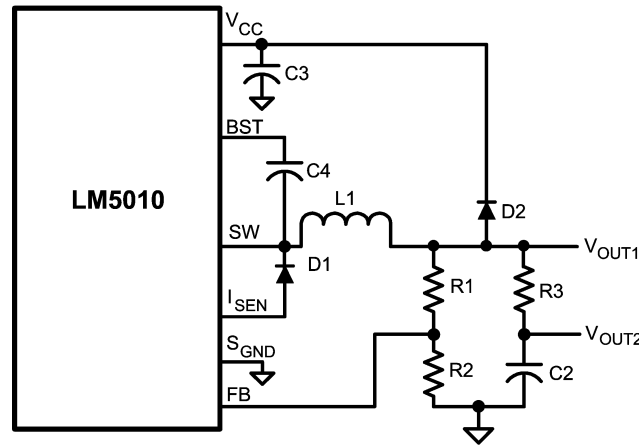
FIGURE 9. Low Ripple Output Configuration

## Start-up Regulator ( $V_{CC}$ )

The startup regulator is integral to the LM5010. The input pin ( $V_{IN}$ ) can be connected directly to line voltages up to 75V. The  $V_{CC}$  output is regulated at 7.0V,  $\pm 6\%$ , and is current limited to 10 mA. Upon power up the regulator sources current into the external capacitor at  $V_{CC}$  (C3). With a 0.1  $\mu$ F capacitor at  $V_{CC}$ , approximately 58  $\mu$ s are required for the  $V_{CC}$  voltage to reach the under-voltage lockout threshold (UVLO) of 5.8V ( $t_1$  in *Figure 8*), at which time the buck switch is enabled, and the softstart pin is released to allow the softstart capacitor (C6) to charge up.  $V_{OUT}$  then increases to its regulated value as the softstart voltage increases ( $t_2$  in *Figure 8*).

The minimum input operating voltage is determined by the regulator's dropout voltage, the  $V_{CC}$  UVLO falling threshold ( $\approx 5.65V$ ), and the frequency. When  $V_{CC}$  falls below the falling threshold the  $V_{CC}$  UVLO activates to shut off the buck switch and ground the softstart pin. If  $V_{CC}$  is externally loaded, the minimum input voltage increases since the output impedance at  $V_{CC}$  is  $\approx 140\Omega$  at low  $V_{IN}$ . See Figures 2 and 3. In applications involving a high value for  $V_{IN}$  where power dissipation in the startup regulator is a concern, an auxiliary voltage can be diode connected to the  $V_{CC}$  pin (*Figure 10*). Setting the auxiliary voltage to between 7.5V and 14V shuts off the internal regulator, reducing internal power dissipation. The current required into the  $V_{CC}$  pin is shown in *Figure 4*. Internally a diode connects  $V_{CC}$  to  $V_{IN}$ .

## Start-up Regulator ( $V_{CC}$ ) (Continued)



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FIGURE 10. Self Biased Configuration

## Regulation Comparator

The feedback voltage at FB is compared to the voltage at the Softstart pin ( $2.5V, \pm 2\%$ ). In normal operation (the output voltage is regulated) an on-time period is initiated when the voltage at FB falls below  $2.5V$ . The buck switch stays on for the on-time causing the FB voltage to rise above  $2.5V$ . After the on-time period the buck switch stays off until the FB voltage falls below  $2.5V$ . Bias current at the FB pin is less than  $5\text{ nA}$  over temperature.

## Over-Voltage Comparator

The feedback voltage at FB is compared to an internal  $2.9V$  reference. If the voltage at FB rises above  $2.9V$  the on-time is immediately terminated. This condition can occur if the input voltage, or the output load, change suddenly. The buck switch will not turn on again until the voltage at FB falls below  $2.5V$ .

## ON-Time Control

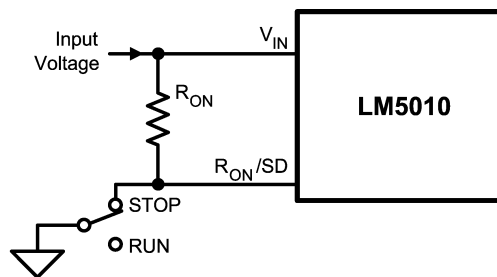
The on-time of the internal switch (see Figure 5) is determined by the  $R_{ON}$  resistor and the input voltage ( $V_{IN}$ ), calculated from the following:

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R_{ON} + 1.4k)}{V_{IN} - 1.4V} + 67\text{ ns} \quad (5)$$

The inverse relationship of  $t_{ON}$  vs.  $V_{IN}$  results in a nearly constant frequency as  $V_{IN}$  is varied. If the application requires a high frequency the minimum value for  $t_{ON}$ , and consequently  $R_{ON}$ , is limited by the off-time ( $265\text{ ns}, \pm 15\%$ ) which limits the maximum duty cycle at minimum  $V_{IN}$ . The tolerance for Equation 5 is  $\pm 25\%$ . Frequencies in excess of  $1\text{ MHz}$  are possible with the LM5010.

## Shutdown

The LM5010 can be remotely shut down by taking the  $R_{ON}/SD$  pin below  $0.65V$ . See Figure 11. In this mode the softstart pin is internally grounded, the on-timer is disabled, and the input current at  $V_{IN}$  is reduced (Figure 7). Releasing the  $R_{ON}/SD$  pin allows normal operation to resume. When the switch is open, the nominal voltage at  $R_{ON}/SD$  is shown in Figure 6.



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FIGURE 11. Shutdown Implementation

## Current Limit

Current limit detection occurs during the off-time by monitoring the recirculating current through the free-wheeling diode (D1). The detection threshold is 1.25A,  $\pm 0.25A$ . Referring to *Figure 1*, when the buck switch is off the inductor current flows through the load, into  $S_{GND}$ , through the sense resistor, out of  $I_{SEN}$  and through D1. If that current exceeds the threshold the current limit comparator output switches to delay the start of the next on-time period. The next on-time starts when the current out of  $I_{SEN}$  is below the threshold and the voltage at FB is below 2.5V. If the overload condition persists causing the inductor current to exceed the threshold during each on-time, that is detected at the beginning of each off-time. The operating frequency is lower due to longer-than-normal off-times.

*Figure 12* illustrates the inductor current waveform. During normal operation the load current is  $I_O$ , the average of the ripple waveform. When the load resistance decreases the

current ratchets up until the lower peak attempts to exceed the threshold. During the Current Limited portion of *Figure 12*, the current ramps down to the threshold during each off-time, initiating the next on-time (assuming the voltage at FB is  $< 2.5V$ ). During each on-time the current ramps up an amount equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L1} \quad (6)$$

During this time the LM5010 is in a constant current mode, with an average load current ( $I_{OCL}$ ) equal to the threshold +  $\Delta I/2$ .

The "valley current limit" technique allows the load current to exceed the current limit threshold as long as the lower peak of the inductor current is less than the threshold.

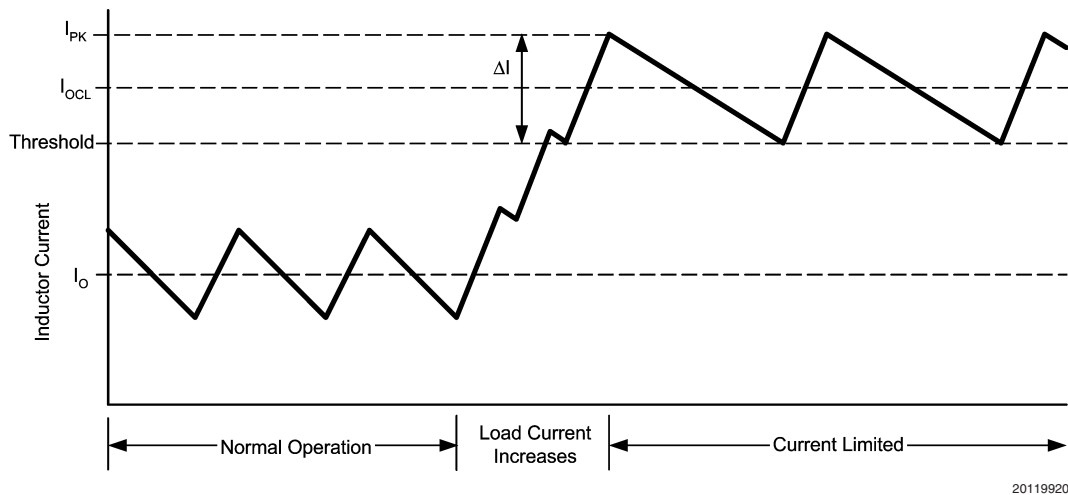


FIGURE 12. Inductor Current - Current Limit Operation

The current limit threshold can be increased by connecting an external resistor ( $R_{CL}$ ) between  $S_{GND}$  and  $I_{SEN}$ . The external resistor typically is less than  $1\Omega$ , and its calculation is explained in the Applications Information section.

The peak current out of SW and  $I_{SEN}$  must not exceed 3.5A. The average current out of SW must be less than 3A, and the average current out of  $I_{SEN}$  must be less than 2A.

## N - Channel Buck Switch and Driver

The LM5010 integrates an N-Channel buck switch and associated floating high voltage gate driver. The peak current through the buck switch must not be allowed to exceed 3.5A, and the average current must be less than 3A. The gate driver circuit is powered by the external bootstrap capacitor between BST and SW (C4). During each off-time, the SW pin is at approximately -1V, and C4 is re-charged from  $V_{CC}$  through the internal high voltage diode. The minimum off-time of 265 ns ensures a minimum time each cycle to recharge the bootstrap capacitor. A 0.022  $\mu F$  ceramic capacitor is recommended for C4.

## Softstart

The softstart feature allows the converter to gradually reach a steady state operating point, thereby reducing startup stresses and current surges. Upon turn-on, after  $V_{CC}$  reaches the under-voltage threshold ( $t_1$  in *Figure 8*), an internal 11.5  $\mu A$  current source charges the external capacitor at the Softstart pin to 2.5V ( $t_2$  in *Figure 8*). The ramping voltage at SS (and at the non-inverting input of the regulation comparator) ramps up the output voltage in a controlled manner. This feature keeps the load current from going to current limit during startup, thereby reducing inrush currents.

An internal switch grounds the Softstart pin if  $V_{CC}$  is below the under-voltage lockout threshold, if a thermal shutdown occurs, or if the circuit is shutdown using the  $R_{ON}/SD$  pin.

## Thermal Shutdown

The LM5010 should be operated so the junction temperature does not exceed  $125^\circ C$ . If the junction temperature increases above that, an internal Thermal Shutdown circuit activates (typically) at  $175^\circ C$ , taking the controller to a low power reset state by disabling the buck switch and the on-timer, and grounding the Softstart pin. This feature helps prevent catastrophic failures from accidental device over-

## Thermal Shutdown (Continued)

heating. When the junction temperature reduces below 155°C (typical hysteresis = 20°C), the Softstart pin is released and normal operation resumes.

## Applications Information

### EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with a design example. The circuit in *Figure 1* is to be configured for the following specifications:

- $V_{OUT} = 10V$
- $V_{IN} = 15V$  to  $75V$
- $F_S = 625$  kHz
- Minimum load current = 150 mA
- Maximum load current = 1.0A
- Softstart time = 5 ms.

**R1 and R2:** The ratio of these resistors is calculated from:

$$R1/R2 = (V_{OUT}/2.5V) - 1 \quad (7)$$

R1/R2 calculates to 3.0. The resistors should be chosen from standard value resistors in the range of 1.0 kΩ - 10 kΩ. Values of 3.0 kΩ for R1, and 1.0 kΩ for R2 will be used.

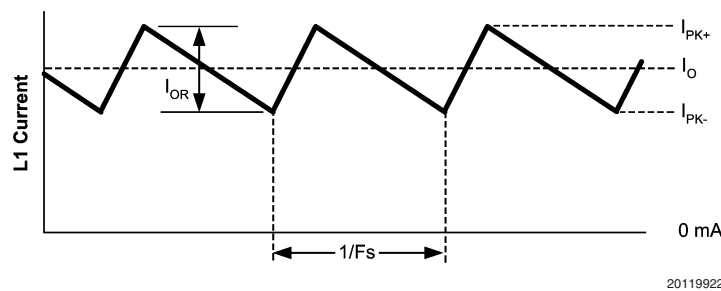


FIGURE 13. Inductor Current

To keep the circuit in continuous conduction mode, the maximum allowed ripple current is twice the minimum load current, or 300 mA p-p. Using this value of ripple current, the inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{I_{OR} \times F_{S(min)} \times V_{IN(max)}} \quad (8)$$

where  $F_{S(min)}$  is the minimum frequency ( $F_S - 25\%$ ).

$$L1 = \frac{10V \times (75V - 10V)}{0.30A \times 463 \text{ kHz} \times 75V} = 63 \mu H$$

This provides a minimum value for L1 - the next higher standard value (100 μH) will be used. L1 must be rated for the peak current ( $I_{PK+}$ ) to prevent saturation. The peak current occurs at maximum load current with maximum ripple. The maximum ripple is calculated by re-arranging Equation 8 using  $V_{IN(max)}$ ,  $F_{S(min)}$ , and the minimum inductor value, based on the manufacturer's tolerance. Assume, for this exercise, the inductor's tolerance is ±20%.

**R<sub>ON</sub>, F<sub>S</sub>:**  $R_{ON}$  sets the on-time, and can be chosen using Equation 2 to set a nominal frequency, or from Equation 5 if the on-time at a particular  $V_{IN}$  is important. A higher frequency generally means a smaller inductor and capacitors (value, size and cost), but higher switching losses. A lower frequency means a higher efficiency, but with larger components. If PC board space is tight, a higher frequency is better. The resulting on-time and frequency have a ±25% tolerance. Re-arranging Equation 2,

$$R_{ON} = \frac{10V}{1.18 \times 10^{-10} \times 625 \text{ kHz}} = 136 \text{ k}\Omega$$

The next larger standard value (137 kΩ) is chosen for  $R_{ON}$ , yielding a nominal frequency of 618 kHz.

**L1:** The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltage ( $V_{IN(min)}$ ,  $V_{IN(max)}$ ). Refer to *Figure 13*.

$$I_{OR(max)} = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{L1_{MIN} \times F_{S(min)} \times V_{IN(max)}} \quad (9)$$

$$I_{OR(max)} = \frac{10V \times (75V - 10V)}{80 \mu H \times 463 \text{ kHz} \times 75V} = 234 \text{ mA p-p}$$

$$I_{PK+} = 1.0A + 0.234A / 2 = 1.117A$$

**R<sub>CL</sub>:** Since it is obvious that the lower peak of the inductor current waveform does not exceed 1.0A at maximum load current (see *Figure 13*), it is not necessary to increase the current limit threshold. Therefore  $R_{CL}$  is not needed for this exercise. For applications where the lower peak exceeds 1.0A, see the section below on increasing the current limit threshold.

**C2 and R3:** Since the LM5010 requires a minimum of 25 mVp-p of ripple at the FB pin for proper operation, the required ripple at  $V_{OUT1}$  is increased by R1 and R2. This necessary ripple is created by the inductor ripple current acting on C2's ESR + R3. First, the minimum ripple current is determined.

## Applications Information (Continued)

$$I_{OR(min)} = \frac{V_{OUT1} \times (V_{IN(min)} - V_{OUT1})}{L1_{MAX} \times F_{S(max)} \times V_{IN(min)}} \\ = \frac{10V \times (15V - 10V)}{120 \mu H \times 772 \text{ kHz} \times 15V} = 36 \text{ mA} \quad (10)$$

The minimum ESR for C2 is then equal to:

$$ESR_{(min)} = \frac{25 \text{ mV} \times (R1 + R2)}{R2 \times I_{OR(min)}} = 2.8 \Omega$$

If the capacitor used for C2 does not have sufficient ESR, R3 is added in series as shown in *Figure 1*. C2 should generally be no smaller than 3.3  $\mu\text{F}$ , although that is dependent on the frequency and the allowable ripple amplitude at  $V_{OUT1}$ . Experimentation is usually necessary to determine the minimum value for C2, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C2 than a non-varying load.

**D1:** The important parameters are reverse recovery time and forward voltage drop. The reverse recovery time determines how long the current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is mainly this diode's voltage (plus the voltage across the current limit sense resistor) which forces the inductor current to decrease during the off-time. For this reason, a higher voltage is better, although that affects efficiency. A reverse recovery time of  $\approx 30 \text{ ns}$ , and a forward voltage drop of  $\approx 0.75\text{V}$  are preferred. The reverse leakage specification is important as that can significantly affect efficiency. Other types of diodes may have a lower forward voltage drop, but may have longer recovery times, or greater reverse leakage. D1 should be rated for the maximum  $V_{IN}$ , and for the peak current when in current limit ( $I_{PK}$  in *Figure 11*) which is equal to:

$$I_{PK} = 1.5\text{A} + I_{OR(max)} = 1.734\text{A}$$

where 1.5A is the maximum guaranteed current limit threshold, and the maximum ripple current was previously calculated as 234 mA p-p. Note that this calculation is valid only when  $R_{CL}$  is not required.

**C1:** Assuming the voltage supply feeding  $V_{IN}$  has a source impedance greater than zero, this capacitor limits the ripple voltage at  $V_{IN}$  while supplying most of the switch current during the on-time. At maximum load current, when the buck switch turns on, the current into  $V_{IN}$  increases to the lower

peak of the output current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into  $V_{IN}$  during this on-time is the load current. For a worst case calculation, C1 must supply this average load current during the maximum on-time. The maximum on-time is calculated using Equation 5, with a 25% tolerance added:

$$t_{ON(max)} = \frac{1.18 \times 10^{-10} \times (137\text{k} + 1.4\text{k}) \times 1.25}{15\text{V} - 1.4\text{V}} + 67 \text{ ns} = 1.57 \mu\text{s}$$

C1 is calculated from:

$$C1 = \frac{I_O \times t_{ON}}{\Delta V} = \frac{1.0\text{A} \times 1.57 \mu\text{s}}{1\text{V}} = 1.57 \mu\text{F}$$

where  $I_O$  is the load current, and  $\Delta V$  is the allowable ripple voltage at  $V_{IN}$  (1V for this example). Quality ceramic capacitors with a low ESR should be used for C1. To allow for capacitor tolerances and voltage effects, a 2.2  $\mu\text{F}$  capacitor will be used

**C3:** The capacitor at the  $V_{CC}$  pin provides not only noise filtering and stability, but also prevents false triggering of the  $V_{CC}$  UVLO at the buck switch on/off transitions. For this reason, C3 should be no smaller than 0.1  $\mu\text{F}$ , and should be a good quality, low ESR, ceramic capacitor. This capacitor also determines the initial startup delay ( $t_1$  in *Figure 8*).

**C4:** The recommended value for C4 is 0.022  $\mu\text{F}$ . A high quality ceramic capacitor with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turn-on. A low ESR also ensures a complete recharge during each off-time.

**C5:** This capacitor suppresses transients and ringing due to long lead inductance at  $V_{IN}$ . A low ESR, 0.1  $\mu\text{F}$  ceramic chip capacitor is recommended, located physically close to the LM5010.

**C6:** The capacitor at the SS pin determines the softstart time, i.e. the time for the reference voltage at the regulation comparator, and the output voltage, to reach their final value. The time is determined from the following:

$$t_{SS} = \frac{C6 \times 2.5\text{V}}{11.5 \mu\text{A}}$$

For a 5 ms softstart time, C6 calculates to 0.022  $\mu\text{F}$ .

### FINAL CIRCUIT

The final circuit is shown in *Figure 14*, and its performance is shown in Figures 15 - 18.

## Applications Information (Continued)

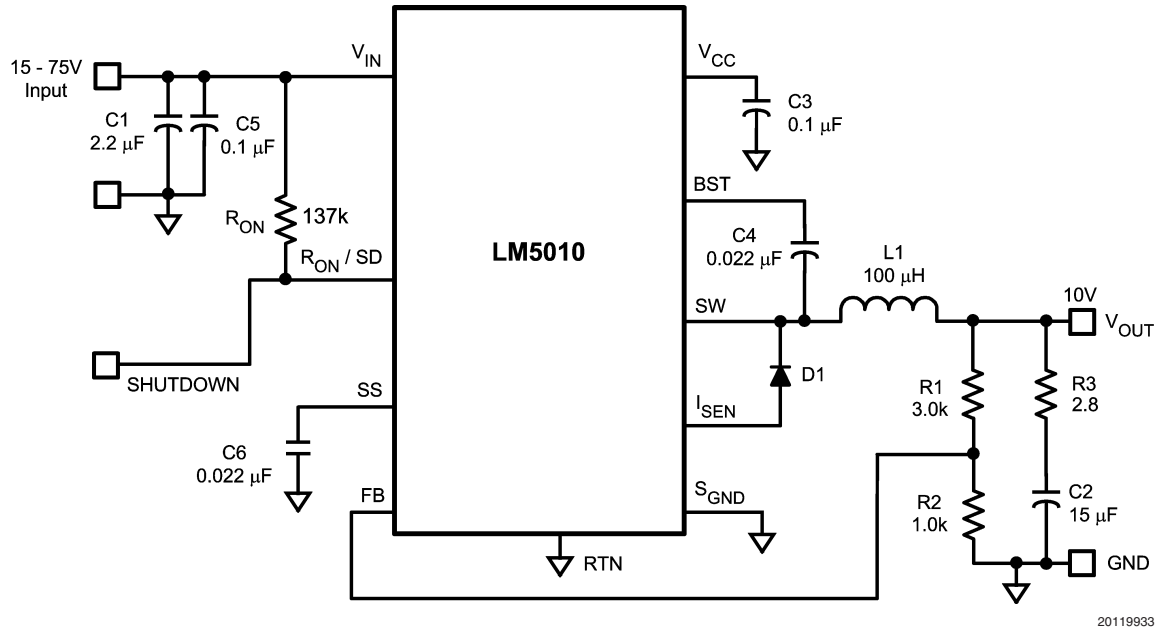
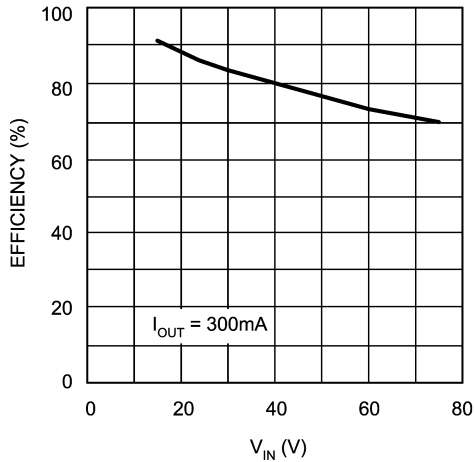


FIGURE 14. LM5010 Example Circuit

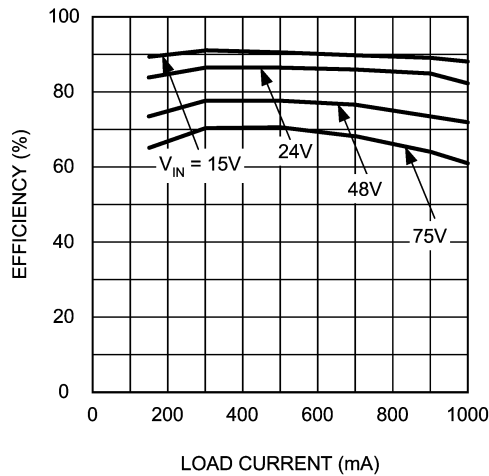
Item	Description	Part No.	Package	Value
C1	Ceramic Capacitor	TDK C4532X7R2A225M	1812	2.2 $\mu$ F, 100V
C2	Ceramic Capacitor	TDK C4532X7R1E156M	1812	15 $\mu$ F, 25V
C3	Ceramic Capacitor	Kemet C0805C104K4RAC	0805	0.1 $\mu$ F, 16V
C4, C6	Ceramic Capacitor	Kemet C0805C223K4RAC	0805	0.022 $\mu$ F, 16V
C5	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 $\mu$ F, 100V
D1	Ultra fast diode	Central Semi CMR2U-01	SMB	100V, 2A
L1	Inductor	TDK SLF10145	10.1 x 10.1	100 $\mu$ H
R1	Resistor	Vishay CRCW08053001F	0805	3.0 $k\Omega$
R2	Resistor	Vishay CRCW08051001F	0805	1.0 $k\Omega$
R3	Resistor	Vishay CRCW08052R80F	0805	2.8 $\Omega$
R <sub>ON</sub>	Resistor	Vishay CRCW08051373F	0805	137 $k\Omega$
U1	Switching regulator	National Semi LM5010		

## Applications Information (Continued)



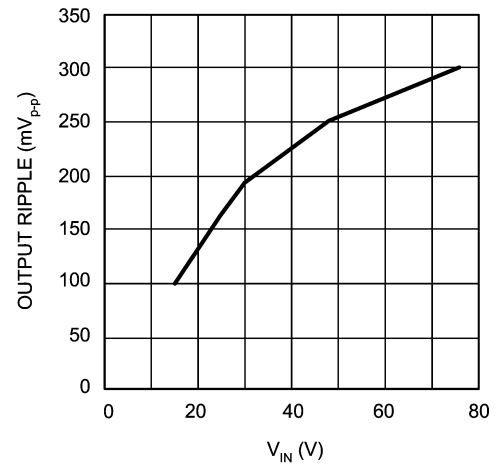
20119934

FIGURE 15. Efficiency vs V<sub>IN</sub>  
Circuit of Figure 14



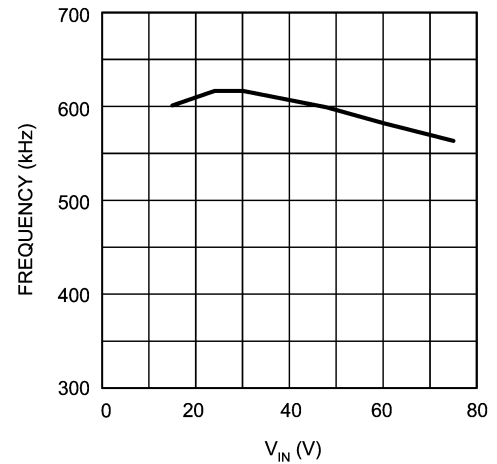
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FIGURE 16. Efficiency vs Load Current and V<sub>IN</sub>  
Circuit of Figure 14



20119936

FIGURE 17. Output Voltage Ripple vs V<sub>IN</sub>  
Circuit of Figure 14



20119937

FIGURE 18. Frequency vs V<sub>IN</sub>  
Circuit of Figure 14

#### INCREASING THE CURRENT LIMIT THRESHOLD

The current limit threshold is nominally 1.25A, with a minimum guaranteed value of 1.0A. If, at maximum load current, the lower peak of the inductor current ( $I_{PK}$  in Figure 13) exceeds 1.0A, resistor  $R_{CL}$  must be added between  $S_{GND}$  and  $I_{SEN}$  to increase the current limit threshold to equal or exceed that lower peak current. This resistor diverts some of the recirculating current from the internal sense resistor so that a higher current level is needed to switch the internal current limit comparator.  $I_{PK}$  is calculated from:

$$I_{PK} = I_{O(max)} - \frac{I_{OR(min)}}{2} \quad (11)$$

where  $I_{O(max)}$  is the maximum load current, and  $I_{OR(min)}$  is the minimum ripple current calculated using Equation 10.  $R_{CL}$  is calculated from:



## Applications Information (Continued)

$$R_{CL} = \frac{1.0A \times 0.11\Omega}{I_{PK-} - 1.0A} \quad (12)$$

where 0.11Ω is the minimum value of the internal resistance from S<sub>GND</sub> to I<sub>SEN</sub>. The next smaller standard value resistor should be used for R<sub>CL</sub>. With the addition of R<sub>CL</sub> it is necessary to check the average and peak current values to ensure they do not exceed the LM5010 limits. At maximum load current the average current through the internal sense resistor is:

$$I_{AVE} = \frac{I_{O(max)} \times R_{CL} \times (V_{IN(max)} - V_{OUT})}{(R_{CL} + 0.11\Omega) \times V_{IN(max)}} \quad (13)$$

If I<sub>AVE</sub> is less than 2.0A no changes are necessary. If it exceeds 2.0A, R<sub>CL</sub> must be reduced. The upper peak of the inductor current (I<sub>PK+</sub>), at maximum load current, is calculated using the following:

$$I_{PK+} = I_{O(max)} + \frac{I_{OR(max)}}{2} \quad (14)$$

where I<sub>OR(max)</sub> is calculated using Equation 9. If I<sub>PK+</sub> exceeds 3.5A, the inductor value must be increased to reduce the ripple amplitude. This will necessitate recalculation of I<sub>OR(min)</sub>, I<sub>PK-</sub>, and R<sub>CL</sub>.

When the circuit is in current limit, the upper peak current out of the SW pin is

$$I_{PK+(CL)} = \frac{1.5A \times (150 \text{ m}\Omega + R_{CL})}{R_{CL}} + I_{OR(MAX)}$$

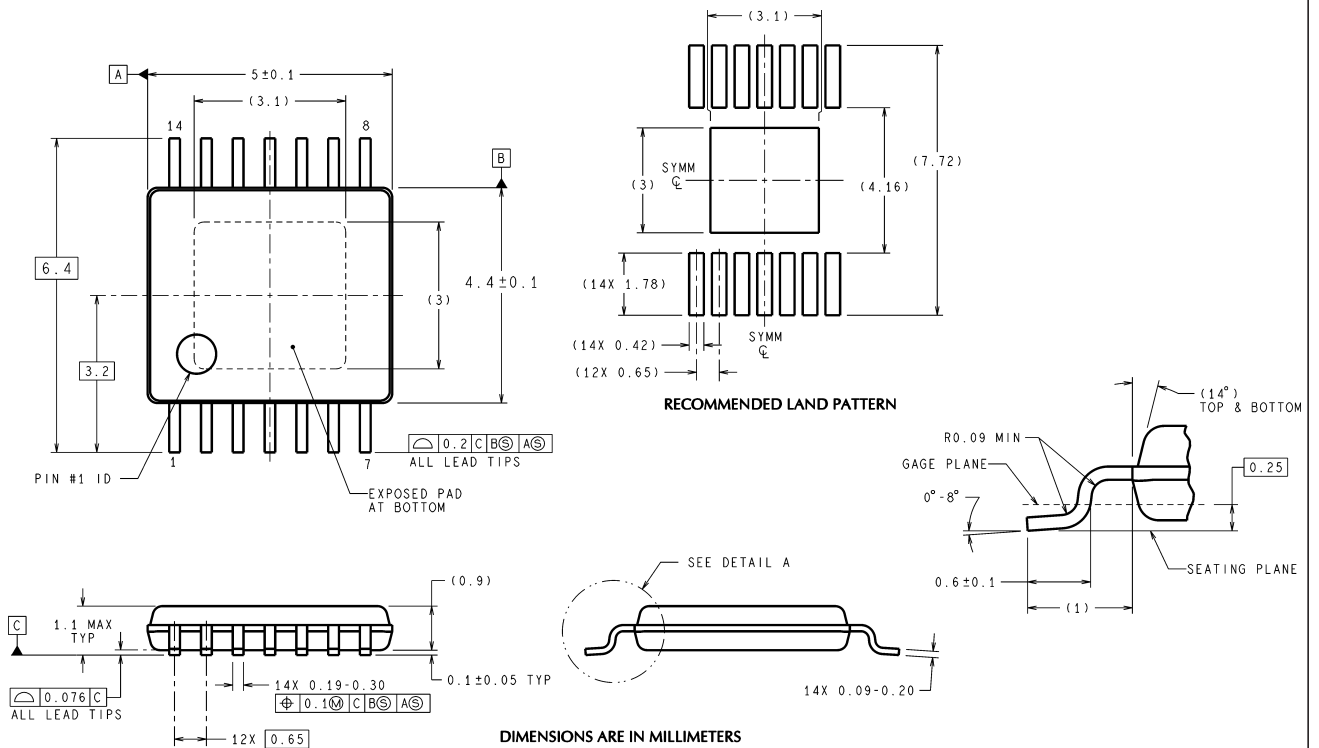
The inductor L1 and diode D1 must be rated for this current.

### PC BOARD LAYOUT

The LM5010 regulation, over-voltage, and current limit comparators are very fast, and will respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all the components must be as close as possible to their associated pins. The current loop formed by D1, L1, C2, and the S<sub>GND</sub> and I<sub>SEN</sub> pins should be as small as possible. The ground connection from C2 to C1 should be as short and direct as possible. If it is expected that the internal dissipation of the LM5010 will produce high junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the IC package bottom can be soldered to a ground plane, and that plane should both extend from beneath the IC, and be connected to exposed ground plane on the board's other side using as many vias as possible. The exposed pad is internally connected to the IC substrate.

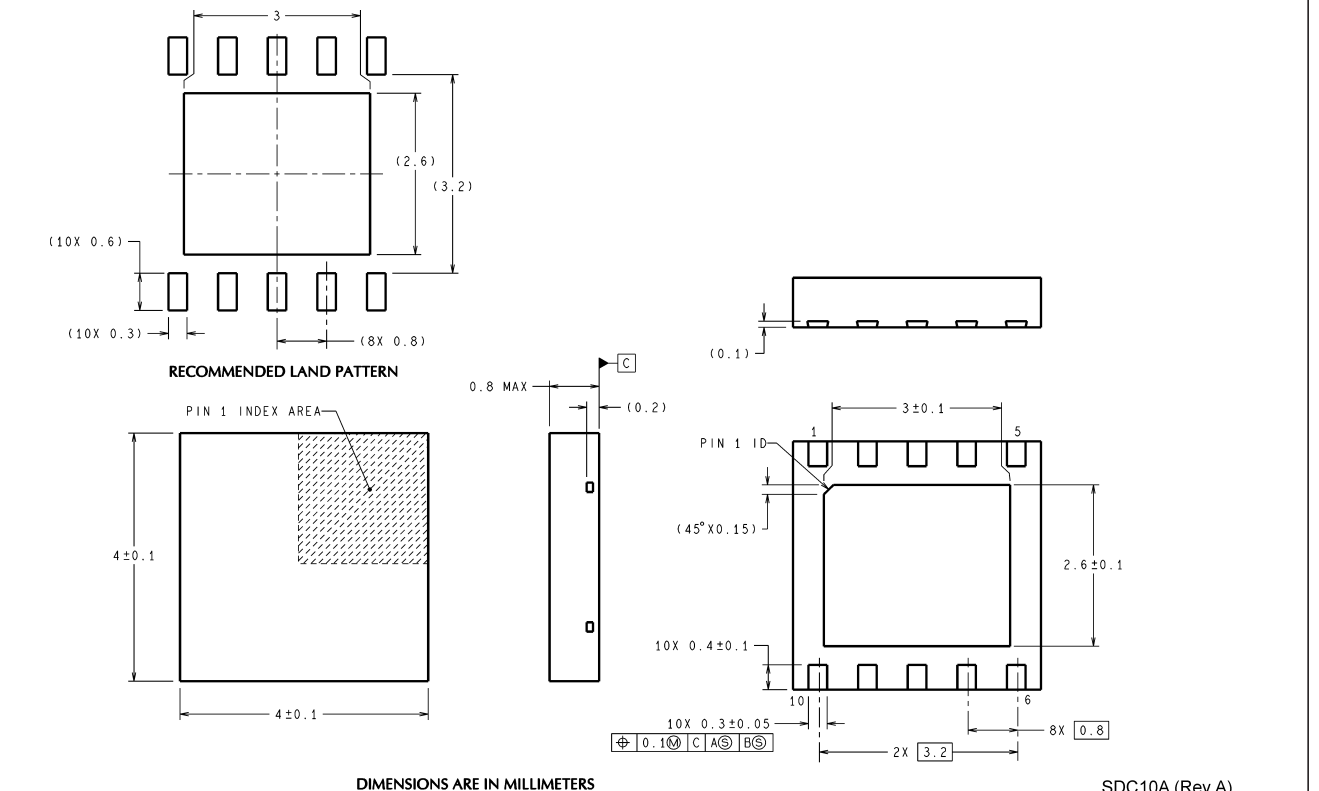
The use of wide PC board traces at the pins, where possible, can help conduct heat away from the IC. The four No Connect pins on the TSSOP package are not electrically connected to any part of the IC, and may be connected to ground plane to help dissipate heat from the package. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

**Physical Dimensions** inches (millimeters) unless otherwise noted



MXA14A (Rev A)

**14-Lead TSSOP Package**  
**NS Package Number MXA14A**



SDC10A (Rev A)

**10-Lead LLP Package**  
**NS Package Number SDC10A**

## Notes

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